Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising:
a central processing unit (CPU);
a bridge coupled to the CPU;
a first slot configured to receive a device, wherein a first portion of the bridge is coupled to the first slot;
a second slot configured to receive a device, wherein a second portion of the bridge is coupled to the second slot;
at least one trace coupled to the first and second slots; and
whereby the computer system is configured so that inserting a jumper board in the first slot couples the first portion of the bridge to the second slot while the jumper board does not occupy the second slot.

2. (Original) The computer system of claim 1, wherein the first and second portions of the bridge comprise a bus.

3. (Currently amended) The computer system of claim 1, wherein each slot is capable of providing all signals pertaining to ~~the~~ a bus.

4. (Currently amended) A computer system, comprising:
a central processing unit (CPU);
a bridge coupled to the CPU;
a first slot configured to receive a device, wherein a first portion of the bridge is coupled to the first slot;
a second slot configured to receive a device, wherein a second portion of the bridge is coupled to the second slot;

at least one trace coupled to the first and second slots; and

whereby the computer system is configured so that inserting a jumper board in the first slot couples the first portion of the bridge to the second slot~~The computer system of claim 1~~, wherein the slots are implemented on a riser board.

5. (Original) The computer system of claim 4, wherein lane polarity inversion techniques are implemented on a printed circuit board that includes the first and second slots.

6. (Original) The computer system of claim 4, wherein lane reversal techniques are implemented on a printed circuit board that includes the first and second slots.

7. (Currently amended) A computer system, comprising:

a central processing unit (CPU);

a bridge coupled to the CPU;

a first slot configured to receive a device, wherein a first portion of the bridge is coupled to the first slot;

a second slot configured to receive a device, wherein a second portion of the bridge is coupled to the second slot;

at least one trace coupled to the first and second slots; and

whereby the computer system is configured so that inserting a jumper board in the first slot couples the first portion of the bridge to the second slot~~The computer system of claim 1~~, wherein the first and second portions of the bridge include a serial bus.

8. (Original) The computer system of claim 7, wherein the serial bus comprises an optical bus.

9. (Original) The computer system of claim 7, wherein the serial bus is a PCI-Express bus.

10. (Original) The computer system of claim 7, wherein the slots do not provide connections for all signals pertaining to the bus without the jumper board.

11. (Currently amended) A method of providing a bus in a computer system, comprising:

routing a first portion of the bus to a first segment of a first slot;

routing a second portion of the bus to a first segment of a second slot;

coupling a second segment of the first slot to a second segment of the second slot; and

inserting a jumper board into the first slot;

wherein the jumper board connects the first and second segments of the first slot, thereby routing the first portion of the bus to the second slot while the jumper board does not occupy the second slot.

12. (Original) The method of claim 11, wherein the first and second portions of the bus comprise the entire bus.

13. (Currently amended) The method of claim 11, further comprising selecting the first and second slots, from among several available slot configurations, to correspond to ~~the width~~ a maximum number of physical lines of the bus.

14. (Currently amended) The method of claim ~~13~~11, further comprising ~~sizing~~ adjusting the first and second slots such that they can physically accommodate more than just the ~~larger than the size of~~ first and second portions.

15. (Original) The method of claim 14, wherein the first and second slots are capable of providing all signals that pertain to the entire bus.

16. (Original) The method of claim 11, wherein the connection between slots occurs on a system board.

17. (Currently amended) A computer system, comprising:
means for allocating a bus among a first and a second slot;
means for coupling a portion of the first slot to a portion of the second slot while not occupying the second slot; and
means for coupling at least two portions of a first slot together;
whereby the second slot is capable of providing the entire bus.

18. (Original) The computer system of claim 17, wherein the means for coupling a portion of the first slot to a portion of the second slot comprises traces on a system board.

19. (Original) The computer system of claim 17, wherein the means for coupling at least two portions of the first slot together comprises a jumper board.

20. (Original) The computer of claim 19, further comprising means for reducing a number of bowtie connections in the system.